Disclosure of the Invention

[0004] Incidentally, for mounting of the aforementioned photodiode array, e.g., a photodiode array for CT, a flat collet or a pyramid collet can be used as a collet for holding a chip under suction. The flat collet is normally used for flip chip bonding. The CT photodiode array has a large chip area (e.g., the square shape of 20 mm on each side). Where the pyramid collet 161 used in an ordinary mounter is used as shown in Fig. 25B, chip 162 will warp due to clearance 163 between chip 162 and pyramid collet 161. For this reason, in the case where the pyramid collet 161 is used, the warpage could cause positional misalignment and degrade the mounting accuracy of chip 162. The flip chip bonding process requires application of heat and pressure, but the efficiency of thermal conduction is poor in use of the pyramid collet 161. The pressure applied could damage the edge of chip 162. From the above it follows that the pyramid collet 161 is not suitable for suction holding of a thin chip. Therefore, in the case of the flip chip bonding, as shown in Fig. 25A, flat collet 160 to achieve surface contact with the chip surface is used to hold the chip 162 under suction, and the heat and pressure from heater block 164 is applied to the chip 162.

[0005] However, the use of the flat collet 160 results in bringing the entire chip surface of the chip 162 into contact with the flat collet 160. If the entire chip surface to become the light incident surface is in contact with the flat collet 160 to be exposed to pressure and heat, regions corresponding to impurity diffused layers forming the photodiodes, on the chip surface could suffer physical damage. The damage on the chip surface will pose problems of appearance failure

and characteristic degradation (increase in dark current and noise or the like).

[0006] The present invention has been accomplished in view of the above-described respects and an object of the invention is to provide a photodiode array and production method thereof capable of preventing the characteristic degradation while preventing the damage on the regions corresponding to the photodiodes during mounting, and to provide a radiation detector.

[0007] In order to achieve the above object, a photodiode array according to the present invention is a photodiode array comprising a semiconductor substrate, wherein a plurality of photodiodes are formed in array on an opposite surface side to an incidence surface of light to be detected, in the semiconductor substrate, and wherein a projection having a predetermined height is provided in a region not corresponding to regions where the photodiodes are formed, on a side of the incidence surface of the light to be detected, in the semiconductor substrate.

[0008] In the photodiode array according to the present invention, the projection projects relative to regions corresponding to the regions where the photodiodes are formed, on the incidence surface side of the semiconductor substrate. In the case where the flat collet is used in mounting, the projection functions as a spacer for forming a clearance relative to the flat collet. For this reason, the flat collet is kept out of direct contact with the regions corresponding to the regions where the photodiodes are formed, whereby the corresponding regions are prevented from being damaged by pressure and heat. In consequence, it is feasible to effectively prevent the characteristic degradation due to

noise, dark current, and so on.

[0009] Preferably, a plurality of depressions having a predetermined depth are formed in array on the opposite surface side to the incidence surface of the light to be detected, in the semiconductor substrate, and each photodiode is formed in a bottom portion of the associated depression. In this case, the distance becomes shorter between the incidence surface of the light to be detected and the photodiodes in the semiconductor substrate, and thus recombination of carriers is suppressed in migration of carriers generated with incidence of the light to be detected. This results in improving photodetecting sensitivity.

[0010] Preferably, the projection is made of a resin or metal having a light blocking property. In this case, the light is prevented from entering the region not corresponding to the regions where the photodiodes are formed, on the incidence surface of the semiconductor substrate. This results in improving the resolution of the photodiode array.

[0011] Preferably, the projection comprises a plurality of projections, and the projections are discontinuously arranged at predetermined intervals. In this case, the projections partition the space in front of the incidence surface of the semiconductor substrate into a plurality of spaces in communication with each other. For this reason, for example, where, for mounting of a scintillator panel described later, a resin is applied to between the scintillator panel and the incidence surface, it becomes easier for the resin to spread into each of the spaces partitioned by the projections. It is also feasible to suppress generation of voids in each space.

[0012] Preferably, the semiconductor substrate is provided with an impurity region between the photodiodes adjacent to each other, for separating the photodiodes from each other. In this case, the impurity region prevents occurrence of surface leak, and thus adjacent photodiodes can be electrically separated from each other with certainty.

[0013] Preferably, a high-impurity-concentration layer of the same conductivity type as the semiconductor substrate is formed on the incidence surface side of the light to be detected, in the semiconductor substrate. In this case, carriers generated near the light-incident surface inside the semiconductor substrate efficiently migrate into each photodiode, without being trapped. This results in enhancing the photodetecting sensitivity.

[0014] A photodiode array production method according to the present invention is a method of producing a photodiode array, the method comprising: a step of preparing a semiconductor substrate comprised of a semiconductor of a first conductivity type; a step of forming a plurality of impurity diffused layers of a second conductivity type on one surface side of the semiconductor substrate to form a plurality of photodiodes each comprised of the impurity diffused layer and the semiconductor substrate, in array; and a step of providing a projection having a predetermined height, in a region not corresponding to regions where the photodiodes are formed, on another surface of the semiconductor substrate.

[0015] The photodiode array production method according to the present invention permits us to obtain the photodiode array wherein the photodiodes are formed in array on one surface of the semiconductor

substrate and wherein the projection is provided in the region not corresponding to the regions where the photodiodes are formed on the other surface.

[0016] Another photodiode array production method according to the present invention is a method of producing a photodiode array, the method comprising: a step of preparing a semiconductor substrate comprised of a semiconductor of a first conductivity type; a step of forming a plurality of depressions in array on one surface side of the semiconductor substrate; a step of forming a plurality of impurity diffused layers of a second conductivity type in bottom portions of the depressions to form a plurality of photodiodes each comprised of the impurity diffused layer and the semiconductor substrate, in array; and a step of providing a projection having a predetermined height, in a region not corresponding to regions where the photodiodes are formed, on another surface of the semiconductor substrate.

[0017] The photodiode array production method according to the present invention permits us to obtain the photodiode array wherein the photodiodes are formed in array in the bottom portions of the depressions formed in one surface of the semiconductor substrate and wherein the projection is provided in the region not corresponding to the regions where the photodiodes are formed, on the other surface.

[0018] Preferably, the method further comprises a step of forming a high-impurity-concentration layer of the first conductivity type on the other surface of the semiconductor substrate, prior to the step of providing the projection. In this case, the high-impurity-concentration layer of the same conductivity type as the semiconductor substrate is

formed on the other surface of the semiconductor substrate. For this reason, carriers generated near the light-incident surface inside the semiconductor substrate efficiently migrate into each photodiode, without being trapped. This results in enhancing the photodetecting sensitivity.

[0019] Preferably, the method further comprises a step of providing an impurity region of the first conductivity type between the impurity diffused layers adjacent to each other. In this case, the method permits us to obtain the photodiode array wherein adjacent photodiodes are electrically separated from each other with certainty.

[0020] A radiation detector according to the present invention is a radiation detector comprising: the above-described photodiode array; and a scintillator panel arranged opposite to the incidence surface of the light to be detected, in the photodiode array, and arranged to emit light with incidence of radiation.

[0021] Another radiation detector according to the present invention is a radiation detector comprising: the photodiode array produced by the above-described photodiode array production method; and a scintillator panel arranged opposite to the surface where the projection is provided in the photodiode array, and arranged to emit light with incidence of radiation.

[0022] Since each of these radiation detectors according to the present invention comprises the above-described photodiode array, it is feasible to effectively prevent the characteristic degradation due to noise, dark current, and so on.

Brief Description of the Drawings

[0023] Fig. 1 is a view showing a sectional configuration of a photodiode array according to the first embodiment.

[0024] Fig. 2 is a view for explaining the configuration of the photodiode array according to the first embodiment.

[0025] Fig. 3 is a view for explaining a production step of the photodiode array according to the first embodiment.

[0026] Fig. 4 is a view for explaining a production step of the photodiode array according to the first embodiment.

[0027] Fig. 5 is a view for explaining a production step of the photodiode array according to the first embodiment.

[0028] Fig. 6 is a view for explaining a production step of the photodiode array according to the first embodiment.

[0029] Fig. 7 is a view for explaining a production step of the photodiode array according to the first embodiment.

[0030] Fig. 8 is a view for explaining a production step of the photodiode array according to the first embodiment.

[0031] Fig. 9 is a view for explaining a production step of the photodiode array according to the first embodiment.

[0032] Fig. 10 is a view for explaining a production step of the photodiode array according to the first embodiment.

[0033] Fig. 11 is a view for explaining a production step of the photodiode array according to the first embodiment.

[0034] Fig. 12A is a plan view schematically showing an example of the photodiode array according to the first embodiment.

[0035] Fig. 12B is a plan view schematically showing an example of the photodiode array according to the first embodiment.

[0036] Fig. 12C is a plan view schematically showing an example of the photodiode array according to the first embodiment.

[0037] Fig. 13A is a plan view schematically showing an example of the photodiode array according to the first embodiment.

[0038] Fig. 13B is a plan view schematically showing an example of the photodiode array according to the first embodiment.

[0039] Fig. 13C is a plan view schematically showing an example of the photodiode array according to the first embodiment.

[0040] Fig. 14 is a view showing a sectional configuration of a photodiode array according to the second embodiment.

[0041] Fig. 15 is a view for explaining the configuration of the photodiode array according to the second embodiment.

[0042] Fig. 16 is a view for explaining a production step of the photodiode array according to the second embodiment.

[0043] Fig. 17 is a view for explaining a production step of the photodiode array according to the second embodiment.

[0044] Fig. 18 is a view for explaining a production step of the photodiode array according to the second embodiment.

[0045] Fig. 19 is a view for explaining a production step of the photodiode array according to the second embodiment.

[0046] Fig. 20 is a view for explaining a production step of the photodiode array according to the second embodiment.

[0047] Fig. 21 is a view for explaining a production step of the photodiode array according to the second embodiment.

[0048] Fig. 22 is a view for explaining a production step of the photodiode array according to the second embodiment.

[0049] Fig. 23 is a view showing a sectional configuration of a radiation detector according to the third embodiment.

[0050] Fig. 24 is a view showing a sectional configuration of a radiation detector according to the fourth embodiment.

[0051] Fig. 25A is a view schematically showing a state in which a flat collet holds a semiconductor chip under suction.

[0052] Fig. 25B is a view schematically showing a state in which a pyramid collet holds a semiconductor chip under suction.

[0053] Fig. 26 is a perspective view showing a photodiode array according to the conventional technology.

[0054] Fig. 27 is a schematic diagram showing a sectional configuration along direction XXVII-XXVII in Fig. 26.

Best Mode for Carrying out the Invention

[0055] The preferred embodiments of the photodiode array and production method thereof, and the radiation detector according to the present invention will be described below in detail with reference to the drawings. The same elements, or elements with the same functionality will be denoted by the same reference symbols in the description, without redundant description.

[0056] (First Embodiment)

Fig. 1 is a view showing a sectional configuration of photodiode array 1 according to an embodiment of the present invention. In the description hereinafter, the incidence surface of light L (the upper surface in Fig. 1) will be referred to as a back surface, and the opposite surface (the lower surface in Fig. 1) to it as a front surface. It is noted that the dimensions in each drawing below are altered as occasion may

demand, for convenience' sake of illustration.

[0057] The photodiode array 1 has a plurality of photodiodes 4 comprised of pn junctions. The plurality of photodiodes 4 are two-dimensionally arranged in a vertically and horizontally regular array on the front surface side of the photodiode array 1. Each photodiode 4 functions as a pixel of photodiode array 1 and the photodiodes 4 as a whole constitute one photosensitive region.

[0058] The photodiode array 1 has an n-type (first conductivity type) silicon substrate 3. The thickness of the n-type silicon substrate 3 is approximately 30-300 μm (preferably, 100 μm). The impurity concentration in the n-type silicon substrate 3 is approximately 1×10^{12}-$10^{15}/cm^3$. P-type (second conductivity type) impurity diffused layers 5 are two-dimensionally arranged in a vertically and horizontally regular array on the front surface side of the n-type silicon substrate 3. The thickness of the p-type impurity diffused layers 5 is approximately 0.05-20 μm (preferably, 0.2 μm). The impurity concentration in the p-type impurity diffused layers 5 is approximately 1×10^{13}-$10^{20}/cm^3$. The pn junctions formed of the p-type impurity diffused layers 5 and the n-type silicon substrate 3 constitute the photodiodes 4. A silicon oxide film 22 is formed on the front surface of the n-type silicon substrate 3. A passivation film 2 is formed on this silicon oxide film 22. The passivation film 2 is made, for example, of SiN or the like.

[0059] Electrode wirings 9 are formed corresponding to the respective p-type impurity diffused layers 5 (photodiodes 4), on the silicon oxide film 22. Each electrode wiring 9 is made of aluminum and has the thickness of about 1 μm. One end of each electrode wiring 9 is

electrically connected through a contact hole formed in the silicon oxide film 22, to the corresponding p-type impurity diffused layer 5. The other end of each electrode wiring 9 is electrically connected through a contact hole formed in the passivation film 2, to a corresponding under bump metal (UBM) 11. A bump electrode 12 of solder is formed on each UBM 11. The UBM 11 and bump electrode 12 are electrically connected to each other.

[0060] The UBM 11 is preferably one achieving strong interface bonding to solder and being capable of preventing diffusion of a solder component into aluminum, and is often constructed in multilayer structure. An example of this multilayer structure is nickel (Ni)-gold (Au) by electroless plating. This structure is obtained by depositing a thick nickel plated layer (3-15 μm) on an aluminum-exposed region and depositing a thin gold plated layer (0.05-0.1 μm) thereon. The gold layer is provided for preventing oxidation of nickel. Other available structures include multilayer structures of titanium (Ti)-platinum (Pt)-gold (Au) and chromium (Cr)-gold (Au) formed by liftoff.

[0061] An accumulation layer 8 as a high-impurity-concentration layer is provided on the back surface side of the n-type silicon substrate 3. The accumulation layer 8 is formed in a substantially uniform depth across almost all the back surface. The accumulation layer 8 has the same conductivity type as the n-type silicon substrate 3 and the impurity concentration thereof is higher than that of the n-type silicon substrate 3. The photodiode array 1 of the present embodiment has the accumulation layer 8, but the photodiode array has the photodetecting sensitivity at a practically acceptable level, without provision of the accumulation layer

8.

[0062] An AR film 24 is formed on the accumulation layer 8, in order to cover and protect the accumulation layer 8 and to suppress reflection of light L. The AR film 24 is made, for example, of SiO_2 and has the thickness of about 0.01 to several μm. The AR film 24 may be formed in a multilayer or complex structure with SiN or with an optical film capable of preventing reflection at a desired wavelength, in addition to SiO_2.

[0063] On the front surface side of the n-type silicon substrate 3, a region where each p-type impurity diffused layer 5 exists is a region where a photodiode 4 is formed (hereinafter referred to as a "formed region"), and the region except for the formed regions constitutes a region where the photodiodes are not formed. A plurality of spacers 6 as projections are provided in a region not corresponding to the formed regions of the respective photodiodes 4 (the region not corresponding to the formed regions will be referred to as a "noncorresponding region") on the AR film 24. The spacers 6 have a predetermined height. The spacers 6 are made of resin, metal, or an insulating material and in a predetermined planar pattern. The spacers 6 project at an appropriate height (thickness) relative to regions corresponding to the formed regions of the respective photodiodes 4 (the regions corresponding to the formed regions will be referred to as "corresponding regions"), on the back surface of the n-type silicon substrate 3.

[0064] An n^+-type impurity region 7 is provided between adjacent p-type impurity diffused layers 5, i.e., between adjacent photodiodes 4 in the n-type silicon substrate 3. The thickness of the n^+-type impurity

region 7 is approximately 0.1-several ten μm. The n^+-type impurity region 7 functions as a separating layer for electrically separating adjacent photodiodes 4 (p-type impurity diffused layers 5) from each other. This can securely electrically separate adjacent photodiodes 4 from each other and reduce crosstalk between photodiodes 4. The photodiode array 1 in the present embodiment, without the n^+-type impurity region 7, possesses the photodetecting characteristics at a practically acceptable level.

[0065] The photodiode array 1 is of extremely thin plate shape, as shown in Fig. 2. The width W1 of photodiode array 1 is approximately 22.4 mm, and the thickness D of photodiode array 1 approximately 0.3 mm. The photodiode array 1 has a number of aforementioned photodiodes 4 (e.g., a two-dimensional array of 256 (16×16) photodiodes). The pitch W2 between adjacent photodiodes 4 (pixels) is approximately 1.4 mm. The photodiode array 1 is a chip of a large area (e.g., 22.4 mm × 22.4 mm). The top illustration in Fig. 2 is one for showing how thin the photodiode array 1 is, and the details of the photodiode array 1 are illustrated only in enlarged views.

[0066] In the photodiode array 1, when light L is incident on the back surface, the incident light L passes through the accumulation layer 8 to reach the pn junctions. Then each photodiode 4 generates carriers according to the incident light. At this time, the accumulation layer 8 prevents the carriers generated near the light-incident surface (back surface) inside the n-type silicon substrate 3 from being trapped at the light-incident surface and the interface to the AR film 24. This permits the carriers to efficiently migrate to the pn junctions and thus enhances

the photodetecting sensitivity of the photodiode array 1. A photocurrent caused by generated carriers is extracted through electrode wiring 9 and UBM 11 connected to each p-type impurity diffused layer 5, and from bump electrode 12. The incident light is detected based on the output from the bump electrode 12.

[0067] In the present embodiment, as described above, the spacers 6 are provided each corresponding to the noncorresponding region of each photodiode 4, on the light-incident surface side of light L (i.e., the back surface side) in the photodiode array 1. In the case where the flip chip bonding is carried out with the flat collet holding the photodiode array 1 under suction, each spacer 6 comes into contact with the flat collet and functions to secure a clearance between the flat collet and the corresponding region of each photodiode 4. In this configuration, thanks to the existence of each spacer 6, the corresponding region of each photodiode 4 is kept out of direct contact with the flat collet. Therefore, the corresponding region of each photodiode 4 gets rid of direct stress due to pressure and direct stress due to heat, so that the accumulation layer 8 in the corresponding region is prevented from suffering physical damage. The photodiodes 4 are thus free of the dark current and noise caused by crystal defects or the like due to such damage. In consequence, the photodiode array 1 is able to perform photodetection with high accuracy (at high S/N ratios).

[0068] In cases except for the flip chip bonding, e.g., in a case where the photodiode array 1 is integrated with a scintillator to be used as a CT sensor, as described later, the scintillator is kept out of direct contact with the corresponding regions, and it is thus feasible to avoid damage

during mounting of the scintillator.

[0069] The spacers 6 are brought into direct contact with the flat collet and exposed to pressure and heat during the flip chip bonding. Therefore, the spacers 6 are preferably made of a material that can protect the corresponding regions of the respective photodiodes 4 from the pressure and heat. For example, where the spacers 6 are made of resin, the material to be used is preferably epoxy resin, polyimide resin, silicone resin, urethane resin, acrylic resin, fluororesin, or one of composite materials of these in view of such conditions as the coefficient of thermal expansion, flexibility, elasticity, or no diffusion of impurity ions into each photodiode 4 with application of heat. The thickness of spacers 6 is preferably approximately 2-30 μm (more preferably, 5-6 μm). When the spacers 6 are made of the resin as described above, the surface protecting effect is enhanced during mounting of the photodiode array 1. Furthermore, the spacers 6 do not affect the electrical characteristics of the photodiodes 4 and production thereof is also easy. Particularly, the polyimide resin is suitable because it has good heat resistance to effectively block heat from the flat collet during mounting. A filler may be added in the resin making the spacers 6 so that the spacers 6 possess the light blocking property.

[0070] Metal may also be used as a material for the spacers 6. In this case, the metal is preferably one having the light blocking property; for example, the material can be selected from Al (aluminum), Au (gold), Ni (nickel), Cr (chromium), Ti, silicides, and so on. The spacers 6 may also be constructed in a multilayer structure of these metals. When the foregoing metals are used for making the spacers 6, the spacers 6 block

incidence of the light to between pixels, so as to improve the resolution of the photodiode array 1. Since they enhance the heat radiating property, it also becomes feasible to suppress noise or malfunction due to heat. This effect becomes prominent depending upon the pattern shape of spacers 6 (the details of which will be described later). For example, where the spacers 6 are comprised of a multilayer structure of Al and Ni plated films, suitable film thicknesses thereof are such that the thickness of the former film is approximately 1 μm and the thickness of the latter film approximately 5 μm.

[0071] Furthermore, the spacers 6 may also be made of an insulating material. In this case, the material for the spacers 6 can be selected from glass (SiO_2), SiN, low-melting glass, and so on.

[0072] Supposing a plan view of the photodiode array 1, the spacers 6 are formed in a predetermined pattern on the surface of the photodiode array 1. The pattern of spacers 6 will be referred to hereinafter as a "planar pattern." Where the spacers 6 are provided in the noncorresponding region, a variety of planar patterns 6a can be contemplated; for example, such conceivable patterns include the planar patterns 6a as shown in Figs. 12A-12C and Figs. 13A-13C.

[0073] In the planar pattern 6a shown in Fig. 12A, the spacers 6 are formed like a lattice, and the lattice-shaped spacers 6 are arranged. In the planar pattern 6b shown in Fig. 12B, each spacer 6 is formed in a short wall shape, and these short wall-shaped spacers 6 are discontinuously arranged at predetermined intervals and at positions except for intersections 13b in the noncorresponding region of each photodiode 4. In the planar pattern 6c shown in Fig. 12C, each spacer

6 is formed in a cross shape, and these cross-shaped spacers 6 are arranged at respective intersections 13b.

[0074] The planar patterns 6a-6c shown in Figs. 12A to 12C all are the patterns where the plurality of spacers 6 are regularly arranged. The planar patterns are not limited to these, but may be irregular patterns. An irregular pattern can be obtained, for example, by irregularly setting the arrangement intervals of the short wall-shaped spacers 6 or the cross-shaped spacers 6.

[0075] In the planar patterns 6a-6c shown in Figs. 12A-12C, a plurality of pixel regions 17 partitioned by the spacers 6 are formed on the surface of the photodiode array 1. In this case, adjacent pixel regions 17 are better to be in communication with each other, without being completely partitioned by the spacers 6. Therefore, the spacers 6 are preferably discontinuously arranged as in the planar patterns 6b, 6c shown in Figs. 12B and 12C.

[0076] In the planar pattern 6d shown in Fig. 13A, a spacer 6 is formed in a frame shape, and this frame-shaped spacer 6 is arranged at the edge of photodiode array 1. The corresponding regions of the photodiodes 4 are surrounded by the frame-shaped spacer 6, so that adjacent pixel regions 17 are in communication with each other. In the planar pattern 6e shown in Fig. 13B, each spacer 6 is formed in a continuous wall shape, and these wall-shaped spacers 6 are arranged at the edge of photodiode array 1. In the planar patterns 6d, 6e, the pixel regions 17 are not partitioned by the spacer or spacers 6.

[0077] In the planar patterns 6b, 6c, 6d, and 6e where adjacent pixel regions 17 are in communication with each other, without being

partitioned, as described above, the clearance between adjacent spacers 6 functions as an escape for resin (e.g., optical resin 35 used in bonding of scintillator panel 31 described later). In applying the resin onto the back surface of photodiode array 1, therefore, voids (air bubbles) are unlikely to be made in the pixel regions 17 (to decrease the number of voids), whereby the applied resin can uniformly spread over each pixel region 17 to be uniformly filled.

[0078] In the planar pattern 6f shown in Fig. 13C, the lattice-shaped spacers 6 and the frame-shaped spacer 6 are continuously formed, so that each pixel region 17 is partitioned off by a spacer 6. In the planar pattern 6f where the spacers 6 have the light blocking property, each pixel region 17 is uniformly partitioned off by the spacer 6, so that the resolution of the photodiode array 1 can be improved.

[0079] Next, a production method of the photodiode array 1 according to the present embodiment will be described below on the basis of Figs. 3 to 11.

[0080] The first step is to prepare an n-type silicon substrate 3 having the thickness of about 150-500 μm (preferably, 350 μm), as shown in Fig. 3. Next, a silicon oxide film (SiO_2) 20 is formed on the front surface and on the back surface of the n-type silicon substrate 3 (cf. Fig. 4).

[0081] Next, the silicon oxide film 20 formed on the front surface of the n-type silicon substrate 3 is patterned with a predetermined photomask to form openings at intended positions for formation of the n^+-type impurity regions 7. Then the n-type silicon substrate 3 is doped with phosphorus through the openings formed in the silicon oxide film 20, to

provide the n^+-type impurity regions 7 in the n-type silicon substrate 3. In the present embodiment, the n^+-type impurity region 7 is also formed on the back surface side of the n-type silicon substrate 3. This step (impurity region forming step) may be omitted if the n^+-type impurity regions 7 are not provided. Subsequently, a silicon oxide film 21 is again formed on the front surface and on the back surface of the n-type silicon substrate 3 (cf. Fig. 5). This silicon oxide film 21 is used as a mask in the subsequent step of forming the p-type impurity diffused layers 5.

[0082] Next, the silicon oxide film 21 formed on the front surface of the n-type silicon substrate 3 is patterned with a predetermined photomask to form openings at intended positions for formation of the respective p-type impurity diffused layers 5. The substrate is doped with boron through the openings formed in the silicon oxide film 21, to form the p-type impurity diffused layers 5 in two-dimensional arrangement of a vertical and horizontal array. This results in forming photodiodes 4 of pn junctions between each p-type impurity diffused layer 5 and n-type silicon substrate 3 in two-dimensional arrangement of a vertical and horizontal array. Each photodiode 4 becomes a portion corresponding to a pixel. Subsequently, a silicon oxide film 22 is again formed on the front surface side of the substrate (cf. Fig. 6).

[0083] Next, the back surface of the n-type silicon substrate 3 is polished up to a predetermined thickness (about 30-300 μm) to obtain the n-type silicon substrate 3 in thin shape (thin plate). Then an n-type ion species (e.g., phosphorus or arsenic) is allowed to diffuse from the back surface of the n-type silicon substrate 3 into the depth of about

0.05 to several ten μm, thereby forming the aforementioned accumulation layer 8 with the impurity concentration higher than that of the n-type silicon substrate 3. Furthermore, thermal oxidation is carried out to form the AR film 24 on the accumulation layer 8 (cf. Fig. 7).

[0084] Next, contact holes extending to the respective p-type impurity diffused layers 5 are formed in the formed regions of the respective photodiodes 4 and in the silicon oxide film 22 by the photoetching technology. Subsequently, an aluminum metal film is formed on the silicon oxide film 22 by evaporation, and thereafter it is patterned with a predetermined photomask to form electrode wirings 9 (cf. Fig. 8).

[0085] Next, spacers 6 are provided on the AR film 24 (cf. Fig. 9).

[0086] In the case where the spacers 6 are made of resin, as shown in Fig. 9, they are formed as follows. First, the resin (spacer resin) as a material of the spacers 6 is applied onto the AR film 24, and the applied resin is spread all over by spin coating or screen printing, and is then cured. Thereafter, a photosensitive resin (photoresist) is applied thereonto, and steps of exposure with a predetermined photomask and development are carried out to form a resist pattern corresponding to the spacers 6. Using the resist pattern thus formed, as a mask, the spacer resin is left in predetermined regions, thereby forming the spacers 6 in the predetermined planar pattern. Alternatively, where the resin of spacers 6 is photosensitive, it can be directly appropriately cured through the steps of exposure with a predetermined photomask and development. By the provision of the spacers 6, the corresponding regions of the photodiodes 4 are kept out of direct contact with the flat

collet in mounting with the flat collet, and are thus protected.

[0087] Where the spacers 6 are made of metal, a coating of the metal as a material of the spacers 6 is formed by such a technique as evaporation, sputtering, or CVD, and the coating is left only in the predetermined regions, using the resist pattern formed as described above, as a mask, to form the spacers 6 in the predetermined planar pattern. In this case, the thickness of the coating may be increased by plating.

[0088] After the formation of spacers 6, an SiN film 25 to become the passivation film 2 is formed on the silicon oxide film 22 so as to cover the electrode wirings 9. The SiN film 25 can be formed by sputtering, plasma CVD, or the like. The passivation film 2 may be one selected from the insulating films of SiO_2, PSG, BPSG, etc., polyimide resin, acrylate resin, epoxy resin, fluororesin, composite films and multilayer films thereof, and so on. The step of forming the passivation film 2 may be carried out before the formation of the spacers 6.

[0089] Next, contact holes are formed at predetermined positions in the SiN film 25 to make electrode extracting portions (cf. Fig. 10). Furthermore, the bump electrodes 12 are to be formed. Where the bump electrodes 12 are of solder, since the solder has poor wettability to aluminum, UBM 11 for intervention between each electrode extracting portion and bump electrode 12 is formed on each electrode extracting portion. Then the bump electrode 12 is formed over each UBM 11 (cf. Fig. 11).

[0090] Through the above steps, the production method permits us to produce the photodiode array 1 capable of performing photodetection with high accuracy, without occurrence of noise due to damage in

mounting.

[0091] The bump electrodes 12 can be made by placing solder on the predetermined UBM 11 by the solder ball mounting method or printing method and reflowing the solder. The bump electrodes 12 are not limited to the solder bumps, but may be gold bumps, nickel bumps, or copper bumps, or may be electroconductive resin bumps containing such metal as an electroconductive filler. The drawings show only the extraction of the anode electrodes, and the cathode (substrate) electrodes can also be similarly extracted from the n^+-type impurity regions 7 (though not shown) in the same manner as the anode electrodes. The drawings show the case where the bump electrodes 12 of the anode electrodes are formed in the areas of the n^+-type impurity regions 7, but the bump electrodes 12 of the anode electrodes may be formed in the areas of the p-type impurity diffused layers 5.

[0092] (Second Embodiment)

Next, the second embodiment of the photodiode array and production method thereof will be described.

[0093] The present embodiment is directed to a photodiode array 41 having an n-type silicon substrate 43 in which depressions 45 are formed on the opposite surface side (front surface side) to the incidence surface of light L, as shown in Fig. 14. Since this photodiode array 41 has common portions to the photodiode array 1, the description below will be given with focus on the differences between them, while omitting or simplifying the description of the common portions.

[0094] In the photodiode array 41, a plurality of depressions 45 are formed in two-dimensional arrangement of a vertically and horizontally

regular array on the front surface side of the n-type silicon substrate 43. Each depression 45 is made by recessing a predetermined region of the n-type silicon substrate 43 so as to make it thinner than the region around it, and the depressions 45 are formed at arrangement intervals of about 1.4-1.5 mm. The aforementioned photodiodes 4 are formed in respective bottom portions 45a of the depressions 45, thereby constituting the photodiode array 41 in which the photodiodes 4 are two-dimensionally arranged in array.

[0095] Each depression 45 is formed with a rectangular opening, for example, in the size of about 1 mm × 1 mm in the front surface of the n-type silicon substrate 43 so that the aperture size gradually decreases from the opening toward the bottom portion 45a (i.e., from the front surface side toward the back surface side). In this configuration, each depression 45 has a slope side surface 45b. The depth from the front surface of the n-type silicon substrate 43 to the bottom portion 45a is, for example, about 50 μm.

[0096] Electrode wirings 9 are formed along side faces 45b and on the silicon oxide film 22. One end of each electrode wiring 9 is electrically connected through a contact hole formed in the silicon oxide film 22, to the corresponding p-type impurity diffused layer 5. The other end of each electrode wiring 9 is electrically connected through a contact hole formed in the passivation film 2, to the corresponding UBM 11. An n^+-type impurity region 7 is provided between adjacent photodiodes 4.

[0097] The accumulation layer 8 is formed on the entire back surface side of the n-type silicon substrate 3. The AR film 24 is formed on the

accumulation layer 8. This accumulation layer 8 and the AR film 24 are similar to those in the aforementioned photodiode array 1. The aforementioned spacers 6 are provided in the noncorresponding region of each photodiode 4 on the AR film 24. The spacers 6 are also similar to those in the aforementioned photodiode array 1.

[0098] The photodiode array 41 is of extremely thin plate shape as shown in Fig. 15. The width W1 of the photodiode array 41 is approximately 22.4 mm, and the thickness D of photodiode array 41 150-300 μm. The photodiode array 41 has a number of such photodiodes 4 (e.g., two-dimensional arrangement of 256 (16×16) photodiodes). The pitch W2 between adjacent photodiodes 4 is approximately 1.4 mm. The photodiode array 41 is a chip of a large area (e.g., 22.4 mm × 22.4 mm). The top illustration in Fig. 15 is one showing how thin the photodiode array 41 is, and the details of the photodiode array 41 are illustrated only in enlarged views.

[0099] In the photodiode array 41 constructed as described above, when light L is incident on the back surface, just as in the case of the photodiode array 1, the incident light L passes through the accumulation layer 8 to reach the pn junctions. Each photodiode 4 generates carriers according to the incident light. Since each pn junction is provided in the bottom portion 45a of depression 45, the distance is shorter between the back surface of the n-type silicon substrate 43 and the pn junction (e.g., approximately 10-100 μm). Therefore, the photodiode array 41 is configured to prevent a situation in which the carriers generated with incidence of light L annihilate through recombination in the process of migration. In consequence, the photodiode array 41 is able to maintain

high detection sensitivity.

[0100] The accumulation layer 8 permits the carriers generated near the light-incident surface (back surface) inside the n-type silicon substrate 3 to efficiently migrate to the pn junctions, without recombination. This permits the photodiode array 41 to have higher photodetecting sensitivity (though the photodiode array 41 of the present embodiment has the detection sensitivity at a practically acceptable level, without provision of the accumulation layer 8).

[0101] A photocurrent caused by generated carriers is extracted through electrode wiring 9 and UBM 11 connected to each p-type impurity diffused layer 5, and from bump electrode 12. The incident light is detected based on the output from bump electrode 12. This is much the same as in the case of the photodiode array 1.

[0102] As described above, the photodiode array 41 of the present embodiment is also provided with the spacers 6 corresponding to the noncorresponding region of each photodiode 4 as the photodiode array 1 was. Where the photodiode array 41 is held in suction by the flat collet to be subjected to the flip chip bonding, the spacers 6 protect the corresponding regions of the respective photodiodes 4 so as to avoid direct contact thereof with the flat collet. Therefore, the corresponding regions of the respective photodiodes 4 are kept out of direct stress due to pressure and direct stress due to heat, whereby the accumulation layer 8 in the corresponding regions is free of physical damage. In the photodiodes 4 there is neither dark current nor noise caused by crystal defects or the like due to such damage. In consequence, the photodiode array 41 is able to perform photodetection with high

accuracy (at high S/N ratios).

[0103] In cases except for the flip chip bonding, for example, in a case where the photodiode array 41 is integrated with a scintillator to be used as a CT sensor, as described later, the scintillator is kept out of direct contact with the corresponding regions and it is thus feasible to avoid damage during mounting of the scintillator.

[0104] Next, a production method of the photodiode array 41 according to the present embodiment will be described on the basis of Figs. 3 to 6 and Figs. 16 to 22.

[0105] First, the steps described with Figs. 3 to 6 are executed in the same manner as in the case of the photodiode array 1. Next, the back surface of the n-type silicon substrate 3 is polished to make the n-type silicon substrate 3 thinner (into a thin plate) before the thickness of the n-type silicon substrate 3 becomes a predetermined thickness. Subsequently, a silicon nitride film (SiN) 26 is formed on the front surface and on the back surface of the n-type silicon substrate 3 by LP-CVD (or plasma CVD), and thereafter the silicon oxide film 22 and silicon nitride film 26 on the front surface side are patterned with a predetermined photomask to form openings at intended positions for formation of the respective depressions 45 (cf. Fig. 16).

[0106] Next, the p-type impurity diffused layer 5 and n-type silicon substrate 3 are removed by alkali etching to form a depression 45 so as to leave a frame peripheral part 5a of p-type impurity diffused layer 5, for each target of a region where the p-type impurity diffused layer 5 is formed, in the front surface of the n-type silicon substrate 3. This results in obtaining an n-type silicon substrate 43. At this time, the

frame peripheral part 5a is formed as a region resulting from diffusion with a p-type impurity, in the edge part of the opening of each depression 45. Each depression 45 comes to have a side face 45b and a bottom portion 45a. The frame peripheral part 5a is not always essential. When the frame peripheral part 5a is formed, it provides the effect of preventing noise and dark current due to damage in the edge part formed by etching for formation of the depressions 45. Figs. 14, 15, and 24 show the example without formation of the frame peripheral part 5a.

[0107] Subsequently, the bottom portion 45a of each depression 45 thus formed is doped with boron or the like. This results in forming a p-type impurity diffused layer 5b in the bottom portion 45a of each depression 45, and the photodiodes 4 comprised of pn junctions of such p-type impurity diffused layers 5b and n-type silicon substrate 43 are formed in two-dimensional arrangement of a vertical and horizontal array. Then a silicon oxide film 22 is formed on the regions not covered by the silicon nitride film 26 formed on the front surface (cf. Fig. 17). At this time, though not shown, the silicon oxide film is also formed on the silicon nitride film 26 formed on the back surface.

[0108] Next, the silicon nitride film 26 formed on the back surface of n-type silicon substrate 43 is removed and thereafter the accumulation layer 8 with the impurity concentration higher than that of the n-type silicon substrate 43 is formed by ion implantation with an n-type ion species (e.g., phosphorus or arsenic). Furthermore, thermal oxidation is conducted to form the AR film 24 on the accumulation layer 8. Thereafter, the silicon nitride film 26 formed on the front surface of the

n-type silicon substrate 43 is removed (cf. Fig. 18).

[0109] Then, in the formed region of each photodiode 4 a contact hole extending up to each p-type impurity diffused layer 5b is formed in the silicon oxide film 22 on the front surface side by photoetching technology. Subsequently, an aluminum metal film is formed on the silicon oxide film 22 by evaporation and thereafter patterned with a predetermined photomask to form the electrode wirings 9 (cf. Fig. 19).

[0110] Next, the spacers 6 are provided on the AR film 24 in the same manner as in the first embodiment (cf. Fig. 20).

[0111] After the formation of spacers 6, an SiN film 25 to become the passivation film 2 is formed on the silicon oxide film 22 so as to cover the electrode wirings 9. The SiN film 25 can be formed by sputtering, plasma CVD, or the like. Subsequently, contact holes are formed at positions corresponding to the respective electrode wirings 9 in the SiN film 25 (cf. Fig. 21). Subsequently, the UBM 11 electrically connected with each electrode wiring 9 through the contact hole is formed by electroless plating or the like in the same manner as in the first embodiment. Then the bump electrode 12 is formed over each UBM 11 (cf. Fig. 22).

[0112] Through the above steps, the production method permits us to produce the photodiode array 41 capable of performing photodetection with high accuracy, without occurrence of the noise and dark current due to damage during mounting. The drawings show only the extraction of the anode electrodes, but the cathode (substrate) electrodes can also be extracted from the n^+-type impurity regions 7 (though not shown) in the same manner as the anode electrodes.

[0113] (Third Embodiment)

Next, a radiation detector according to the third embodiment will be described.

[0114] Fig. 23 is a view showing a sectional configuration of radiation detector 50 according to the present embodiment. This radiation detector 50 has a scintillator panel 31 arranged to emit light with incidence of radiation, and the aforementioned photodiode array 1. The scintillator panel 31 emits light generated with incident radiation, from its light exit surface 31a. The scintillator panel 31 is arranged opposite to the light-incident surface of photodiode array 1, i.e., opposite to the surface with the spacers 6 in the photodiode array 1. When the light emerging from the light exit surface 31a of scintillator panel 31 is incident on the light-incident surface, the photodiode array 1 converts the incident light into electric signals.

[0115] The scintillator panel 31 is mounted on the back surface side (incidence surface side) of the photodiode array 1. Since the photodiode array 1 is provided with the aforementioned spacers 6, the back surface of the scintillator panel 31, i.e., the light exit surface 31a is kept out of direct contact with the corresponding regions of the photodiodes 4. The space between the light exit surface 31a of the scintillator panel 31 and the photodiode array 1 created by the spacers 6 is filled with an optical resin 35 having a refractive index set so as to sufficiently transmit the light. This optical resin 35 allows the light from the scintillator panel 31 to efficiently enter the photodiode array 1. This optical resin 35 can be selected from epoxy resin, acrylic resin, urethane resin, silicone resin, fluororesin, etc. with the property of

transmitting the light from the scintillator panel 31, or may be one of composite materials of these resins.

[0116] In an operation of bonding the photodiode array 1 onto an unrepresented mounting wiring board, the flat collet holds the photodiode array 1 under suction. However, since the photodiode array 1 is provided with the aforementioned spacers 6, the sticking surface of the flat collet is kept out of direct contact with the corresponding regions of the respective photodiodes 4. When the scintillator panel 31 is mounted, its light exit surface 31a is not in direct contact with the corresponding regions of the photodiodes 4, either. Therefore, the radiation detector 50 having such photodiode array 1 and scintillator panel 31 is able to prevent occurrence of noise, dark current, etc. due to damage of the corresponding regions in the mounting. In consequence, the radiation detector 50 is able to accurately perform photodetection and, in turn, to accurately perform radiation detection.

[0117] (Fourth Embodiment)

Next, a radiation detector according to the fourth embodiment will be described.

[0118] Fig. 24 is a view showing a sectional configuration of radiation detector 55 according to the present embodiment. This radiation detector 55 has a scintillator panel 31, and the aforementioned photodiode array 41. The scintillator panel 31 is arranged opposite to the light-incident surface of photodiode array 41, i.e., opposite to the surface where the spacers 6 are provided in the photodiode array 41.

[0119] The scintillator panel 31 is mounted on the back surface side (incidence surface side) of the photodiode array 41. Since the

photodiode array 41 is provided with the aforementioned spacers 6, the back surface of the scintillator panel 31, i.e., the light exit surface 31a is kept out of direct contact with the corresponding regions of the photodiodes 4. The space between light exit surface 31a of scintillator panel 31 and photodiode array 1 created by the spacers 6 is filled with the optical resin 35. This optical resin 35 allows the light from the scintillator panel 31 to efficiently enter the photodiode array 41.

[0120] In an operation of bonding the photodiode array 41 to an unrepresented mounting wiring board, the flat collet holds the photodiode array 41 under suction. However, since the photodiode array 41 is provided with the aforementioned spacers 6, the sticking surface of the flat collet is not in direct contact with the corresponding regions of the respective photodiodes 4. When the scintillator panel 31 is mounted, its light exit surface 31a is also kept out of direct contact with the corresponding regions of the photodiodes 4. Therefore, the radiation detector 55 having such photodiode array 41 and scintillator panel 31 is able to prevent occurrence of noise, dark current, etc. due to damage of the corresponding regions in the mounting. In consequence, the radiation detector 55 is able to accurately perform photodetection and, in turn, to accurately perform radiation detection.

[0121] The invention accomplished by the Inventors was specifically described above on the basis of the embodiments thereof, but the present invention is by no means intended to be limited to the above embodiments. For example, the spacers 6 may be provided directly on the n-type silicon substrate 3, 43, or may be provided through a structure such as the AR film 24.

Industrial Applicability

[0122] The present invention is applicable to X-ray CT scanners and radiographic image taking systems.